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Abstract

Method for controlled synchronization to an astable clock
system, and reception unit corresponding thereto

Soft synchronization using a slight change in the
period duration of the clock signal (a) produced makes it
possible to alter said clock signal such that a phase
difference (c) between the stable clock signal (b)
produced by a PLL (6) upon a synchronization signal (S)
and the clock signal (a) produced for the application (4)
is slowly reduced until the two clock signals (a, b) are
in synchronism with one another after a certain time. This
means that the clock signals a produced largely keep their
period duration, so that there is the assurance that
applications called cyclically with this clock pulse can
be executed to the full extent with the necessary degree
of accuracy. By virtue of fluctuations in the period
duration of the first clock transmitter which are
corrected by the PLL (6) being mapped onto the second
clock transmitter, a phase difference (c) which is to be
compensated for remains constant. The process of soft
synchronization thus barely differs from the normal
operating state.

Figure 3